



# Instigate

Parallel Systems Development



## Design Services ◦ EDA SW R&D

### Introduction

Instigate offers a wide range of comprehensive consulting and R&D services for designing multi-tier EDA specific software systems stretching from business requirements to technical specification due to a well trained team with good communication and technology skills. Instigate follows the complete understanding of Customer's operational needs to provide technology solutions without economizing any effort to gain an optimal result. Our services range from requirements and use-case analysis to generation of a proposal and real development. The existing and proven IP allows us to significantly reduce the effort for EDA specific software development. The quality assurance is provided along with the development, that includes test-planning, acceptance criteria, automated regression test-harness creation and test-suite implementation.

### ESL design environment

- Generic TLM 1.0/2.0 simulator engine
- Rich parametric module generators with export to
  - OSCI SystemC, Octave
  - NVIDIA CUDA, AMD ATI Brook
  - Verilog, VHDL
- Co-simulation with the third party HDL simulators, Octave, SystemC
- Co-simulation with NVIDIA and AMD ATI video-cards
- GUI debugger, Profiler, Platform editor

### Front-end for ANSI C/C++/OSCI SystemC to RTL producer

- Optimization for power consumption
- C/C++ and SystemC parsing
- Abstract Syntax Tree (AST) creation
- Instrumentation/back-annotation from/to AST
- Control Data Flow Graph (CDFG) creation
- CDFG optimization

### Custom Memory generator

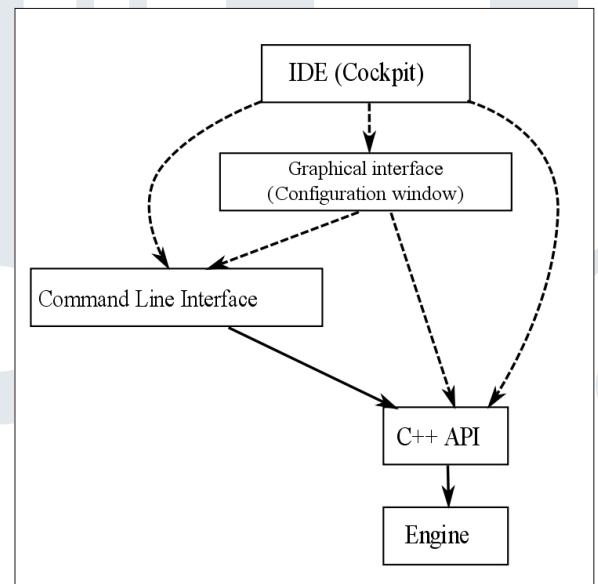
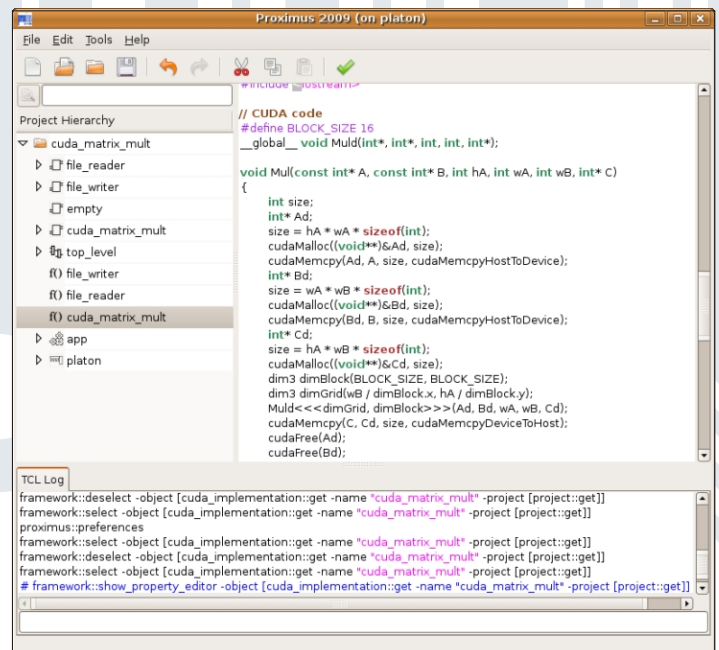
- GUI front-end allowing to specify the parameters of desired memory
- Memory construction using limited HW resources of a proprietary architecture
- Export to Verilog, VHDL, EDIF

### IP-XACT package generation tool

- GUI front-end
- Import/export IP-XACT, Verilog, VHDL

### Module generator

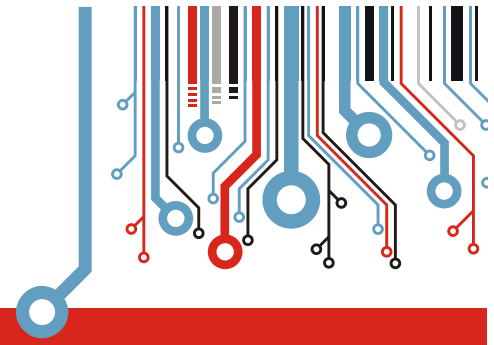
- Graphical User Interface
- Efficient engine in C++
- C++ API: link from GUI to engine
- Command line API
- Export to HDL





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### IDEs for massive parallel reconfigurable architecture

- Clock/bit accurate simulator
- Fast TLM simulator
- Schematic browser/editor: hierarchic netlist viewer with placement/routing
- Profiler: reporting of statistics, bottleneck points, overloaded/free paths
- GUI debugger: data inspection, break points, step-by-step simulation
- Platform editor
  - custom platform creation
  - automatic/manual mapping
  - platform based simulation
- C compiler: C to proprietary programmable HW language

### Methodology

#### Extreme Programming

- Focus on Customer target
  - Interactive specification and scheduling
  - User stories and joint release planning
- Test Driven Development
  - Only create as much code as can be tested
  - Unit Testing (programmer verifies correctness of code)
  - Acceptance tests (based on user stories)
- Linear development
  - All the teams work on the main branch
  - Continuous build and test system to maintain quality

#### Defensive Programming

- Assertion-based Verification and Testing
- No Unverified Assumptions
  - Every function tests all the assumptions
- Pro-Active Catching of Errors
  - Clearly spell out assumption
- Active Comments instead of a regular comment
- Complements unit-tests for complex algorithms

#### Literate Programming

- Documentation as Part of Programming
  - No check-in without documentation
  - Specific rules what, how to document
  - Documentation is embedded in Code
- Documentation Checked by Build System
  - Using Doxygen
  - Missing/bad documentation stops build
- Automatically Generate HTML, PDF, TeX
  - Cross-referenced and linked to code

